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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,048	06/19/2003	Louis A. Lippincott	884.899US1	6019

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2628	

DATE MAILED: 04/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,048	LIPPINCOTT, LOUIS A.	
	Examiner	Art Unit	
	Hau H. Nguyen	2628	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/07/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Terminal Disclaimer

1. The terminal disclaimer filed on February 7, 2006 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Response to Arguments

2. Applicant's arguments filed February 07, 2006 have been fully considered but they are not persuasive. In response to Applicant's argument that reference Barker et al. does not teach the PME (processor memory element) including a processing element, the examiner disagrees. In fact, under the glossary of terms defined by Barker et al., the term PME refers to a single processor, memory and I/O capable system element or unit that forms one of the parallel array processors (col. 7, lines 40-52). Accordingly, reference Barker meets the criteria of the claimed invention. In response to Applicant's argument that reference Barker et al. does not teach a logical connection among the PMEs, the examiner also disagrees. On column 12, lines 28-49, Barker et al. teach each PME has a plurality of input and output ports, which operate in different modes. Normal Mode--Used to transfer data between two adjacent PMEs. Circuit Switched Mode--Allows data and controls to pass through a PME. Zipper Mode--Used by the Array Controller to load or read data from the nodes in a cluster.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5

USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, since each PME as taught by Barker et al. includes processor in its generic form, Wilson, which is related to Barker et al. in parallel processing of array processors, teach the processors are image processors, it would have been obvious to one of ordinary skill in the art at the time the present invention was made to replace the generic processor of Barker which performs generic data operations by any well known specific digital signal processor, such as, the image processor of Wilson in order to perform the specific image process operations because replace one type of processor by another in the same place is considered within the level of ordinary skill in the art.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Barker et al (5,617,577 hereinafter "Barker").

As per claim 1, Barker teaches an apparatus (Fig. 2) comprising a first processor (one of the PME, such as +Z) having a first processor element and at least one I/O port within a first port ring (one of the external ports, 22, 23, 26); and a second processor (one of the PME, such as, +X) having a second processor element and at least one I/O port within a second port ring (one of the external ports, 22, 23, 26), wherein the second processor is coupled to the first processor through

at least one I/O port of a third ring of a third processor (one of the PME, such as, +Y). Therefore, at least claim 1 is anticipated by Barker.

As per claim 2, Barker teaches the at least one I/O port of the first processor is not directly connected to the at least one I/O port of the second processor (such as, external port connects between processor +Z and +W instead of +X).

As per claim 3, the first processor, the second processor and the third processor are part of a number of processors in a point-to-point configuration (col. 12, lines 18-27).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4-12 and 18-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barker et al (5,617,577 hereinafter "Barker") in view of Wilson (5,557,734).

As per claim 1, Barker teaches an apparatus (Fig. 2) comprising a number of image signal processors (PMEs) coupled together in a point-to-point configuration (col. 12, lines 18-27), wherein one image signal processor of the number of image signal processors includes at least one processor element (one of the PME, such as +Z) and a port ring (one of the external ports, 22, 23, 26), wherein the port ring includes a number of ports (such as, I/O ports), a port of the number of ports coupled to the other ports of the port ring and to a port of a port ring (one of the external ports, 22, 23, 26) of a different image signal processor (one of the PME, such as, +X). It

is noted that Barker fails to explicitly teach or suggest the processor is an image signal processor and performing image process-based operations. Wilson teaches a parallel processing system comprising a plurality of processors connected in a ring network (Fig. 1, 26) for processing image data (Fig. 1, 25). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to replace the generic processor of Barker which performs generic data operations by any well known specific digital signal processor, such as, the image processor of Wilson in order to perform the specific image process operations because replace one type of processor by another in the same place is considered within the level of ordinary skill in the art. Therefore, at least claim 7 would have been obvious.

As per claim 4, the combined system teaches the first processor is configured to transmit output from an image process operation to the second processor through the at least one I/O port of the port ring of the third processor based on a logical connection (Barker, Fig. 2, and col. 12, lines 1-18, any one of the PME can indirectly connects to any other PME via any number of intermediate PMEs and Wilson, Fig. 1, 25).

As per claim 5, Barker teaches the at least one I/O port within the port ring of the first processor , the at least one I/O port within the port ring of the second processor and the at least one I/O port within the port ring of the third processor comprise a FIFO memory (Fig. 4, 82).

As per claim 6, Barker teaches the at least one port of the first processor, the at least one port of the second processor and the at least one port of the third processor comprise a receiver port (input ports) and a transmitter port (output port) , wherein the first processor is configured to transmit the output based on a handshake protocol among the receiver ports and the transmitter

ports of the first processor, the second processor and the third processor (Fig. 2, col. 12, lines 18-27).

As per claim 8, the combined system teaches the at least one processor element in a first of the number of image processors is configured to perform one of a number of image processed-based operations (one of the processors).

Claims 9 and 10 are similar in scope to claim 4, and thus are rejected under similar rationale.

As per claim 11, Barker teaches the logical connections are to originate at a source image signal processor (such as, a first processor) and traverse a number of intermediate image signal processors (in between PMEs) of the number of image signal processors and to complete at a destination image signal processor (last PME) of the number of image signal processors, wherein the source image signal processor is transmit an initialize signal, prior to transmission of data along the logical connection, through the number of intermediate image signal processors to the destination image signal processor in the order that data is transmitted in the logical connection (see Fig. 2 and col. 12, lines 1-18).

Claim 12 is similar in scope to claim 5, and thus is rejected under similar rationale.

Claims 18-21 are similar in scope to claims 7-12, and thus are rejected under similar rationale.

Claims 22-24, 25-27 and 28-30 are also similar in scope to claims 7-12, and thus are rejected under similar rationale.

7. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barker et al (5,617,577 hereinafter "Barker") in view of Wilson (5,557,734) and Poplin (us2003/0063213).

The teachings of Barker and Wilson are given in previous paragraph of this Office action. Barker further teaches a host processor (Fig. 1, 1), a host memory (2), a number of expansion interfaces (such as, external port from +Z, -Z, etc ..., also see Fig. 3B). However, the combined system fails to explicitly teach or suggest a CMOS sensor to capture image data. This is what Poplin teaches (Fig. 1, 112). Poplin teaches a digital image device (102) comprising an image sensor (112) and an image processor (114) and a host system (104) comprising a host processor (124) and host memory (120) and an image capturing parameter adjuster (122). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of CMOS image sensor of Poplin into the combined system of Barker and Wilson because CMOS image sensor provides high speed video capturing and thus further increase the overall image processing performance. Therefore, at least claim 13 would have been obvious.

As per claim 14, Barker teaches the at least one image signal processor comprises a hardware accelerator (PME) to execute image process operations.

As per claim 15, Barker teaches the image processor comprises a global bus (such as, bus connects to BCI 21 in Fig. 2) coupled to the number of expansion interfaces and the number of image signal processors, independent of the point-to-point configuration among the number of image signal processors.

Claim 16 is similar in scope to claim 11, and thus is rejected under similar rationale.

As per claim 17, Barker teaches traversal through the number of ports of the port rings of the at least one intermediate image signal processor is independent of image process operations by processor elements within the at least one intermediate image signal processors (col. 12, lines 1-18).

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kee Tung can be reached on (571) 272-7794.

The fax number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

H. Nguyen

04/26/2006

Kee M. Tung
Primary Examiner